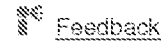



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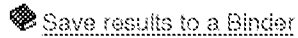
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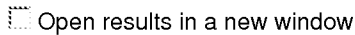
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Angelos Bilas, Jaswinder Pal Singh

November 1997 Supercomputing '97: Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)

Publisher: ACM

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Keywords: bandwidth, clustering, communication parameters, distributed memory, host overhead, interrupt cost, latency, network occupancy, shared memory

2 [Overshadow: a virtualization-based approach to retrofitting protection in commodity operating systems](#)

Xiaoxin Chen, Tal Garfinkel, E. Christopher Lewis, Pratap Subrahmanyam, Carl A. Waldspurger, Dan Boneh, Jeffrey Dvoskin, Dan R.K. Ports

March 2008 ASPLOS XIII: Proceedings of the 13th international conference on Architectural support for programming languages and operating systems

Publisher: ACM

 Full text available: [pdf\(272.32 KB\)](#)

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Commodity operating systems entrusted with securing sensitive data are remarkably large and complex, and consequently, frequently prone to compromise. To address this limitation, we introduce a virtual-machine-based system called Overshadow that protects ...

Keywords: VMM, cloaking, hypervisors, memory protection, multi-shadowing, operating systems, virtual machine monitors

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Mashhuda Glencross, Alan G. Chalmers, Ming C. Lin, Miguel A. Otaduy, Diego Gutierrez

July 2006 SIGGRAPH '06: ACM SIGGRAPH 2006 Courses

Publisher: ACM

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Keywords: collaborative environments, haptics, high-fidelity rendering, human-computer interaction, multi-user, networked applications, perception, virtual reality

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Interrupt register bits should be cleared by writing a high value back to the ... This requires the creation of an interrupt hierarchy with lower level ...

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S & T registers Memory Hierarchy Fast vs big run time vs compile time ... mask context priority polling (interrupt)/ spin-waiting interrupt enable bit ...

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The bit will remain set until the End of Interrupt register is written to by the processor. The ISR register may have multiple bits set if higher priority ...

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[Multiple interrupt handling method and apparatus - Patent 6272585](#)

5410708, April, 1995, Miyamori, 395/725, Multi-register interrupt controller with multiple interrupt detection capability ...

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Enable/Disable Interrupt Bit; Kernel/User mode to protect when can Disable Interrupt; Register showing cause of interrupt; PC address of interrupted ...

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Multiple Interrupts. Disable interrupts while an interrupt is being processed ... Sets appropriate bits in the I/O status register; No interrupts occur ...

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Probably the best way to view the soft interrupt masks is as extensions of the hardware interrupt masks: it's as if the mask register has 64 bits instead of ...

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to multiple interrupts, traps and operating modes. Control timing is with 32-bit products being accumulated in a 64-bit register. ...

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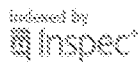
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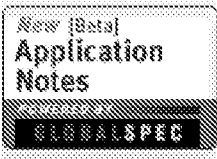
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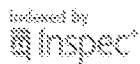
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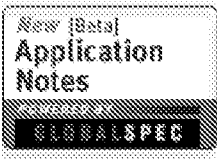
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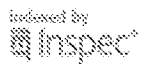
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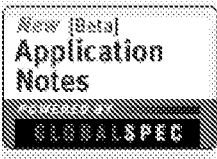
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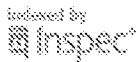
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